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first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second clock signal input/output line, wherein the first and second inverters function to reduce the skew present in the complementary clock input signal. ✓

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16. (Twice Amended) A circuit for reducing clock signal skew comprising:

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at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second internal complementary clock signals, wherein the at least first and second complementary clock signals have a time lag skew relative to each other;

a first N-channel transistor coupled to a second N-channel transistor, a gate of said first N-channel transistor coupled to receive said second clock input signal, and said second N-channel transistor coupled to receive said first clock input signal;

a first P-channel transistor coupled to a second P-channel transistor, a gate of said first P-channel transistor coupled to receive said second clock input signal, and said second P-channel transistor coupled to receive said first clock input signal;

said second N-channel transistor coupled in series to said second P-channel transistor and said first clock signal input/output line connected between said second N-channel transistor and said second P-channel transistor; and

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said first N-channel transistor coupled in series to said first P-channel transistor and said second clock signal input/output line connected between said first N-channel transistor and said first P-channel transistor, wherein the transistors operate to output the at least first and second complementary clock signals with a reduced skew.

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26. (Twice Amended) A circuit for reducing signal skew comprising:

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at least a first and second complementary clock signal input/output line for receiving first and second complementary clock input signals and transmitting first and second complementary clock output signals, wherein the complementary clock input signals have a skewed time lag relative to each other;

first and second inverters each having an input and an output, said input of said first inverter connected to said output of said second inverter and to said first clock signal input/output line and said input of said second inverter connected to said output of said first inverter and to said second, complementary clock signal input/output line wherein the first and second inverters operate to reduce the skew present in the complementary clock input signals; and a first and second driver circuit, said first and second driver circuit connected to said first and second clock signal input/output lines, respectively.

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82. (Amended) A method of generating an internal clock signal in an integrated circuit, the method comprising the steps of:

receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other; and

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modifying the transition of one of said external clock signals relative to the other to produce, from said external clock signals, internal clock signals which have reduced skew.

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91. (Amended) A method of generating an internal clock signal in an integrated circuit, the method of comprising the steps of:

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receiving first and second external clock signals, wherein the second external clock signal is an inverse of the first external clock signal and where there exists a time lag skew of one of said external clock signals relative to the other;

buffering each of the first and second external clock signals using a reference voltage;

modifying the transition of one of said buffered external clock signals relative to the other to produce, from said buffered external clock signals, internal clock signals which have reduced skew.
